

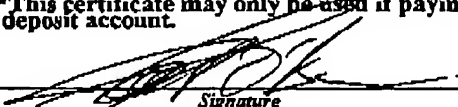
**TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT**  
(Under 37 CFR 1.97(b) or 1.97(c))Docket No.  
**BOW5075.04A**In Re Application Of: **Robert W. Bower**Serial No.  
**10/033,715**Filing Date  
**12/28/2001**Examiner  
**S. A. Gebremariam**Group Art Unit  
**8633**Title: **LIGHT EMISSION FROM SEMICONDUCTOR INTEGRATED CIRCUITS**Address to:  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450**37 CFR 1.97(b)**

1. ☐ The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

**37 CFR 1.97(c)**

2. ☒ The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

☐ the statement specified in 37 CFR 1.97(e);**OR**☒ the fee set forth in 37 CFR 1.17(p).

<b>TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT</b> (Under 37 CFR 1.97(b) or 1.97(c))			Docket No. <b>BOWS075.04A</b>
In Re Application: <b>Robert W. Bower</b>			
Serial No. <b>10/033,715</b>	Filing Date <b>12/28/2001</b>	Examiner <b>S. A. Gebremariam</b>	Group Art Unit <b>8633</b>
<b>LIGHT EMISSION FROM SEMICONDUCTOR INTEGRATED CIRCUITS</b>			
<b>Payment of Fee</b> (Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))			
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<p>I certify that this document and authorization to charge deposit account is being facsimile transmitted to the United States Patent and Trademark Office (Fax No. _____) on _____ (Date)</p> <p style="text-align: center;">_____ Signature</p> <p style="text-align: center;">_____ Typed or Printed Name of Person Signing Certificate</p>		<p>I certify that this document and fee is being deposited on _____ with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.</p> <p style="text-align: center;">_____ Signature of Person Mailing Correspondence</p> <p style="text-align: center;">_____ Typed or Printed Name of Person Mailing Certificate</p>	
<p>*This certificate may only be used if paying by deposit account.</p> <div style="display: flex; justify-content: space-between;"><div style="width: 45%;"><p style="text-align: center;">_____ Signature</p><p><b>John P. O'Banion, Reg. No. 33,201</b> <b>O'BANION &amp; RITCHEY LLP</b> 400 Capitol Mall, Suite 1350 Sacramento, CA 95814 (916) 498-1010</p></div><div style="width: 45%; text-align: right;"><p>Dated: <b>09 April 2004</b></p></div></div>			
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PTO/SB/08B (08-03)

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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

**Complete if Known**

Application Number	10/033,715
Filing Date	12/28/2001
First Named Inventor	Robert W. Bower
Art Unit	8633
Examiner Name	S. A. Gebremariam
Attorney Docket Number	BOW5075.04A

Sheet 1

of 1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		Ellis, R. K. et al. "Electron Tunneling in Non-planar Floating Gate Memory Structure", IDEM, 1982, pp. 749-752.	
		Shealy, J.R. et al. "Direct band gap structures on nanometer-scale, micromachined silicon tips", Appl. Phys. Lett. Vol. 70, No. 25, June 1997, pp. 3458-3460.	
		Prickett, B.L. et al. "Trapping in Tunnel Oxides Grown on Textured Polysilicon", 21st annual Proceedings on Reliability Physics, 1983, pp. 114-117.	
		Dimitrijević, S. "Understanding Semiconductor Devices", Oxford Press, New York, ISBN 019513186X, 2000, Chapter 8, Photonic Devices, Fig. 8.10.	
		Neamen, D. "Semiconductor Physics & Devices - Basic Principles", second edition, ISBN 0256242143, 1997, p. 67.	
		Mayer, J.W. "Electronic Materials Science: For Integrated Circuits in Si and GaAs", Macmillan Publishing, ISBN 0-02-378140-8, 1989, Section 14.8, pp. 431-436.	
		Grove, A.S. "Physics and Technology of Semiconductor Devices", John Wiley and Sons, ISBN 0471329983, 1967, pp. 128-129.	
		Sze, S.M. "Physics of Semiconductor Devices", Wiley-Interscience, ISBN 0471056618, 1981, pp. 46, 47, 690, 691.	
		Wegener, H.A.R. et al. "The prediction of textured poly floating gate memory endurance", 23rd annual Proceedings on Reliability Physics, 1985, pp. 11-17.	

Examiner Signature	Date Considered
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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